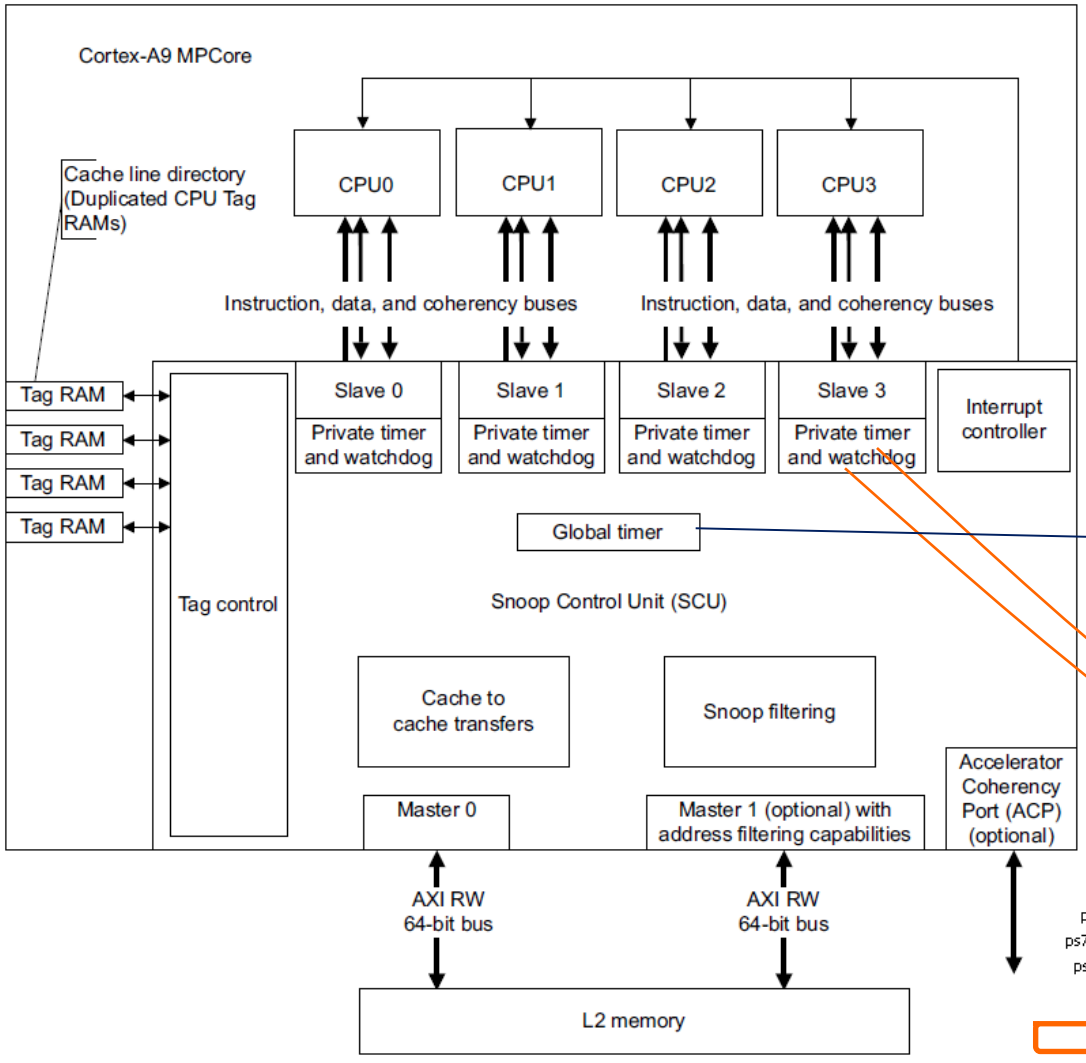
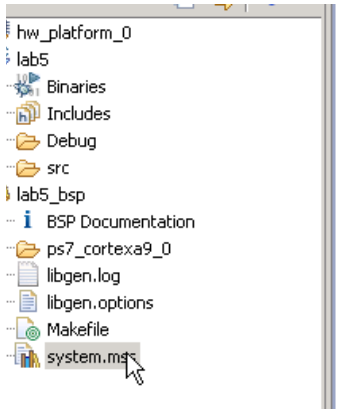
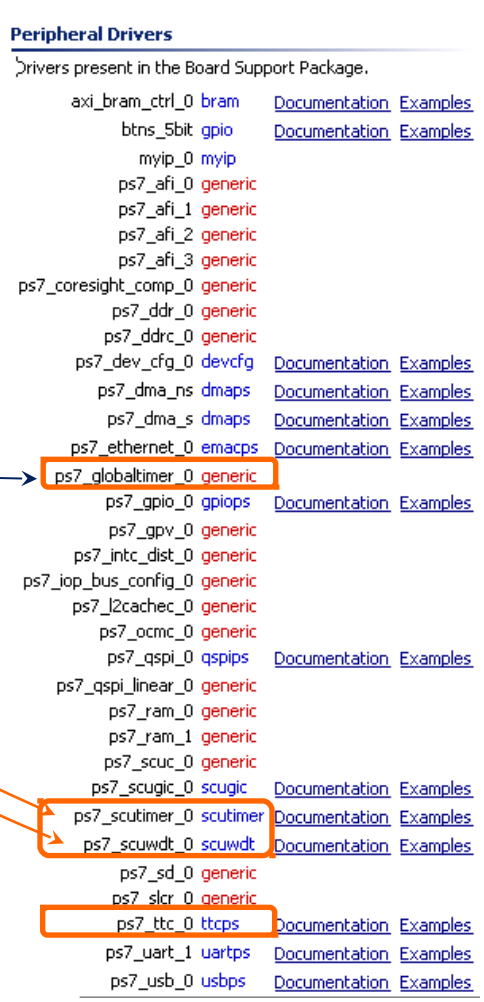
Cortex-A9 MPcore







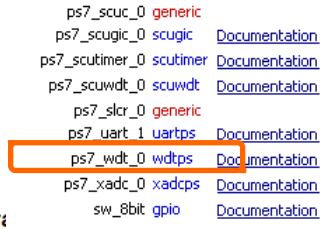


Figure 1-1 Example multiprocessor configura

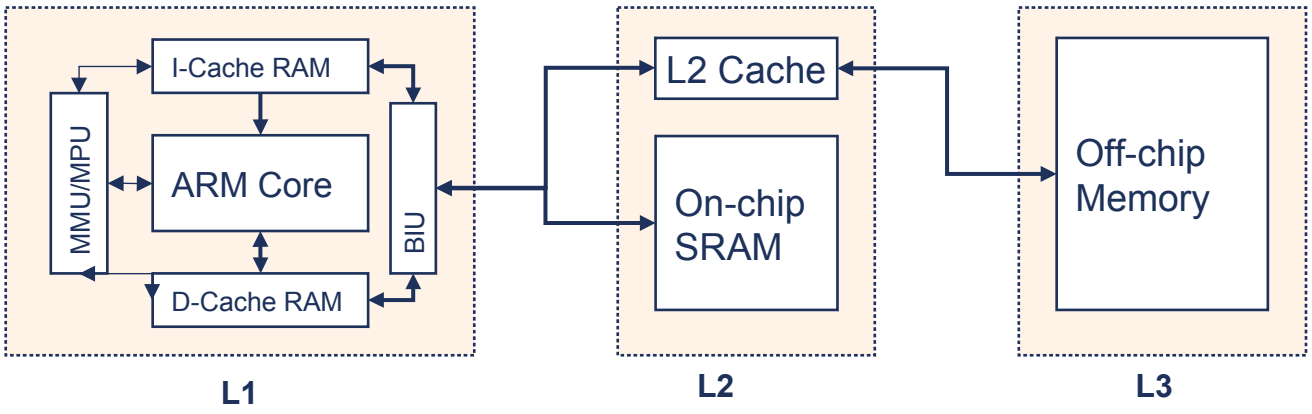
ARM Cortex-A9 note

- 處理器之間可透過 IPI (Inter-Processor Interrupt) 溝通
- 處理器之間是合作關係，彼此沒有從屬的關係
- 所有的處理器都看到同樣的記憶體空間，彼此所定址的實體記憶體空間也是一樣
  - 在同樣的記憶體位置上都是存取同樣的記憶體內容
  - 共同基於同一個作業系統程式碼，來對所有的處理器進行 Task 的排程工作
- 所有的處理器都共享同樣的 I/O 周邊與中斷控制器，每個處理器都可以收到來自任何周邊的中斷觸發

Memory Types

- **The memory type controls the following:**
  - Memory access ordering rules
  - Caching and buffering behaviour
- **There are 3 mutually exclusive memory types:**
  - Normal
  - Device
  - Strongly Ordered
- **Normal and Device memory allow additional attributes for specifying**
  - The cache policy
  - Whether the region is Shared
  - Normal memory allows you to separately configure Inner and Outer cache policies

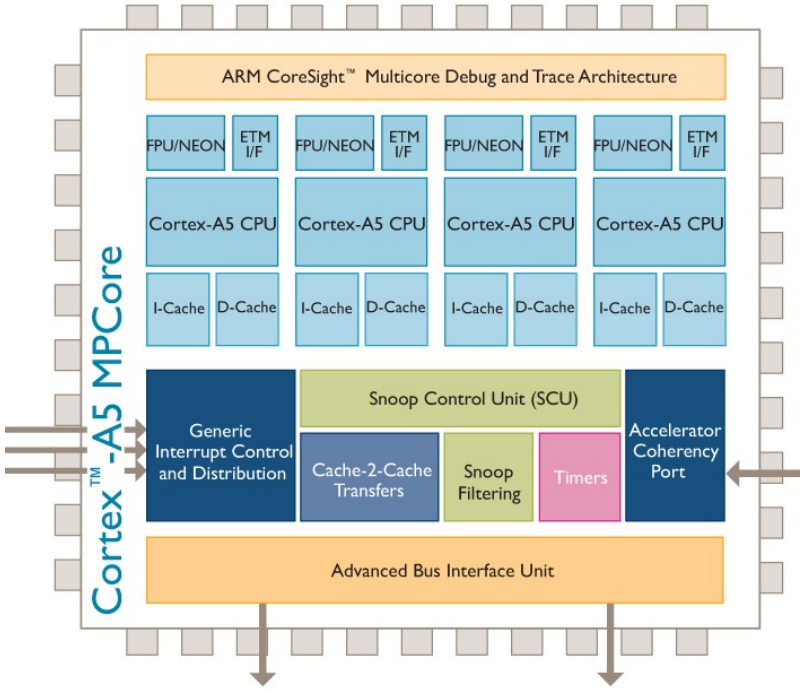
L1 and L2 Caches

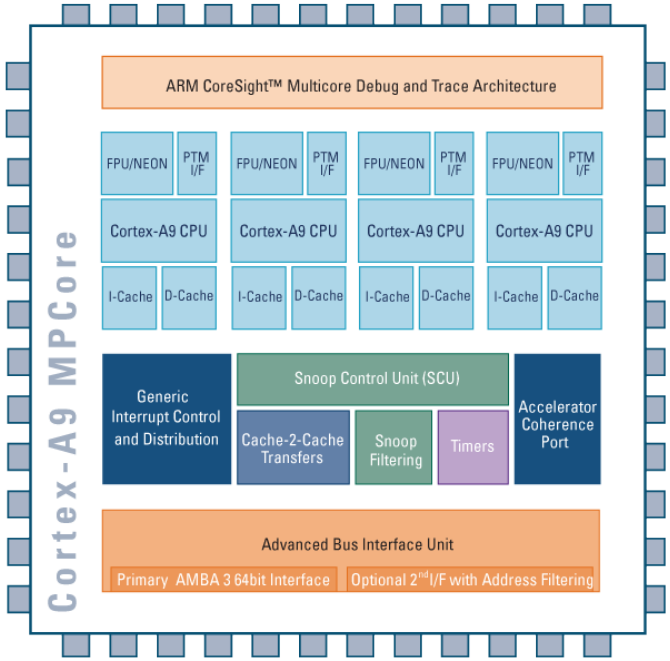


- **Typical memory system can have multiple levels of cache**
  - Level 1 memory system typically consists of L1-caches, MMU/MPU and TCMs
  - Level 2 memory system (and beyond) depends on the system design
- **Memory attributes determine cache behavior at different levels**
  - Controlled by the MMU/MPU (discussed later)
  - Inner Cacheable attributes define memory access behavior in the L1 memory system
  - Outer Cacheable attributes define memory access behavior in the L2 memory system (if external) and beyond (as signals on the bus)
- **Before caches can be used, software setup must be performed**

Cortex MPCore Processors

- **Standard Cortex cores, with additional logic to support MPCore**
  - Available as 1-4 CPU variants
- **Include integrated**
  - Interrupt controller
  - Snoop Control Unit (SCU)
  - Timers and Watchdogs

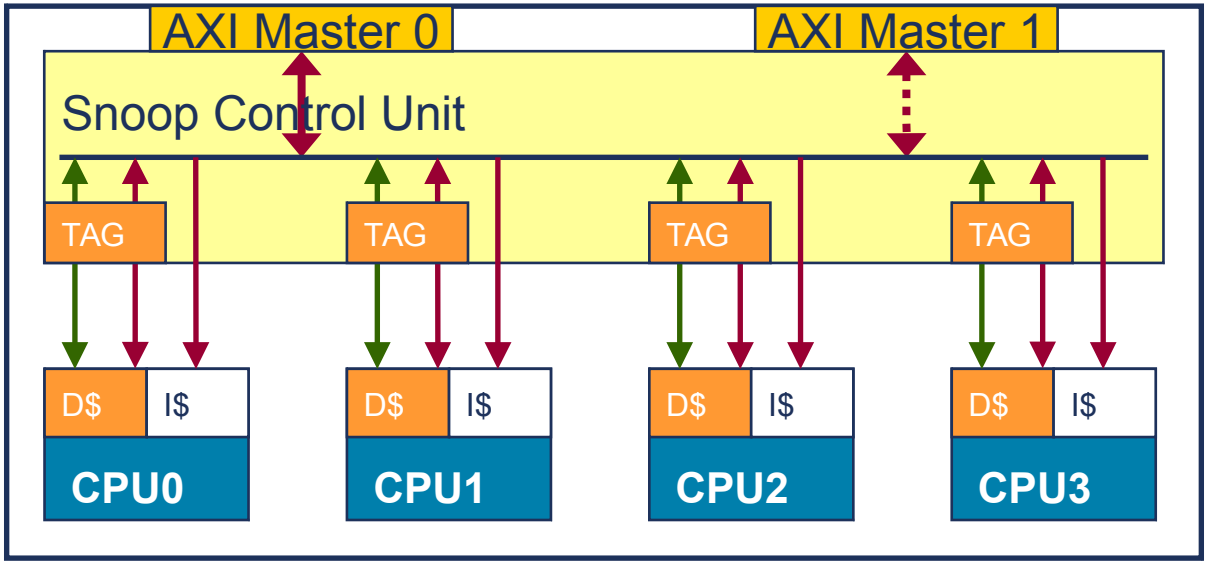




Snoop Control Unit

- **The Snoop Control Unit (SCU) maintains coherency between L1 data caches**
  - Duplicated Tag RAMs keep track of what data is allocated in each CPU's cache
    - Separate interfaces into L1 data caches for coherency maintenance
  - Arbitrates accesses to L2 AXI master interface(s), for both instructions and data

- **Optionally, can use address filtering**
  - Directing accesses to configured memory range to AXI Master port 1



SCU note

- 主要用以連結 1-4 個 MPCore 處理器 , 透過 AXI Bus 去存取 Memory system, 主要功能包括
  - 同步每個 MPCore 處理器的 Data Cache 內容 (不包括 Instruction Cache 的同步)
  - 初始化 L2 Cache 與 AXI Memory Access 的行為
  - 仲裁每個 MPCore 處理器對 L2 Cache 的存取行為
  - 管理 ACP(Accelerator Coherency Port) 介面的存取
- ACP(Accelerator Coherency Port) 主要用於連接原本不被處理器 cache 管理的 AXI Master 週邊 , 例如 DMA Engine

ACP note

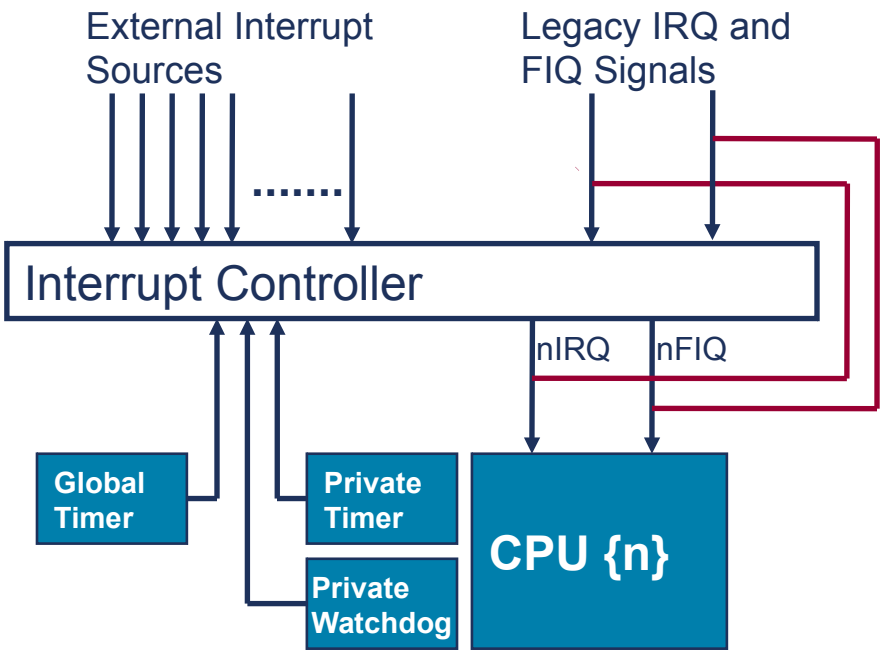
- 若用 DMA 搬了一塊記憶體，而 CPU 不知情 (因為不是透過 CPU 搬), 那麼 CPU 就不能用 cache memory 來存取這塊記憶體，以免發生預期以外的狀況。而既然不能 cache, 於是 CPU 就不能自由地操作
- 一般來說，部分的 DMA 還是透過 CPU 填寫 register, 故 CPU 可以等 DMA 完成，然後再進行一般的操作。不過在多工的情況下，使用起來就會更加地麻煩

ACP note

- ARM 的 ACP 就是解決上述問題
- 假如一個裝置被掛在 ACP 上，那麼即使用 DMA 對這個裝置進行操作，其內容也會被同步到 cache memory 裡面，包括 L1 和 L2 cache
  - 雖然 ACP 只支援 3 -bit 的 AXI device ID， 也就是 8 個裝置，但可用 bridge 的方式加以擴充
  - device read 時，依序在 L1, L2 cache 和 external memory 讀資料；device write 時，會優先更新 L1 cache, 並 invalid 舊資料，當然也就更新 L2 cache
- 若有很多 DMA, 又有很多 CPU 動作，那麼 ACP 可以更快，省電

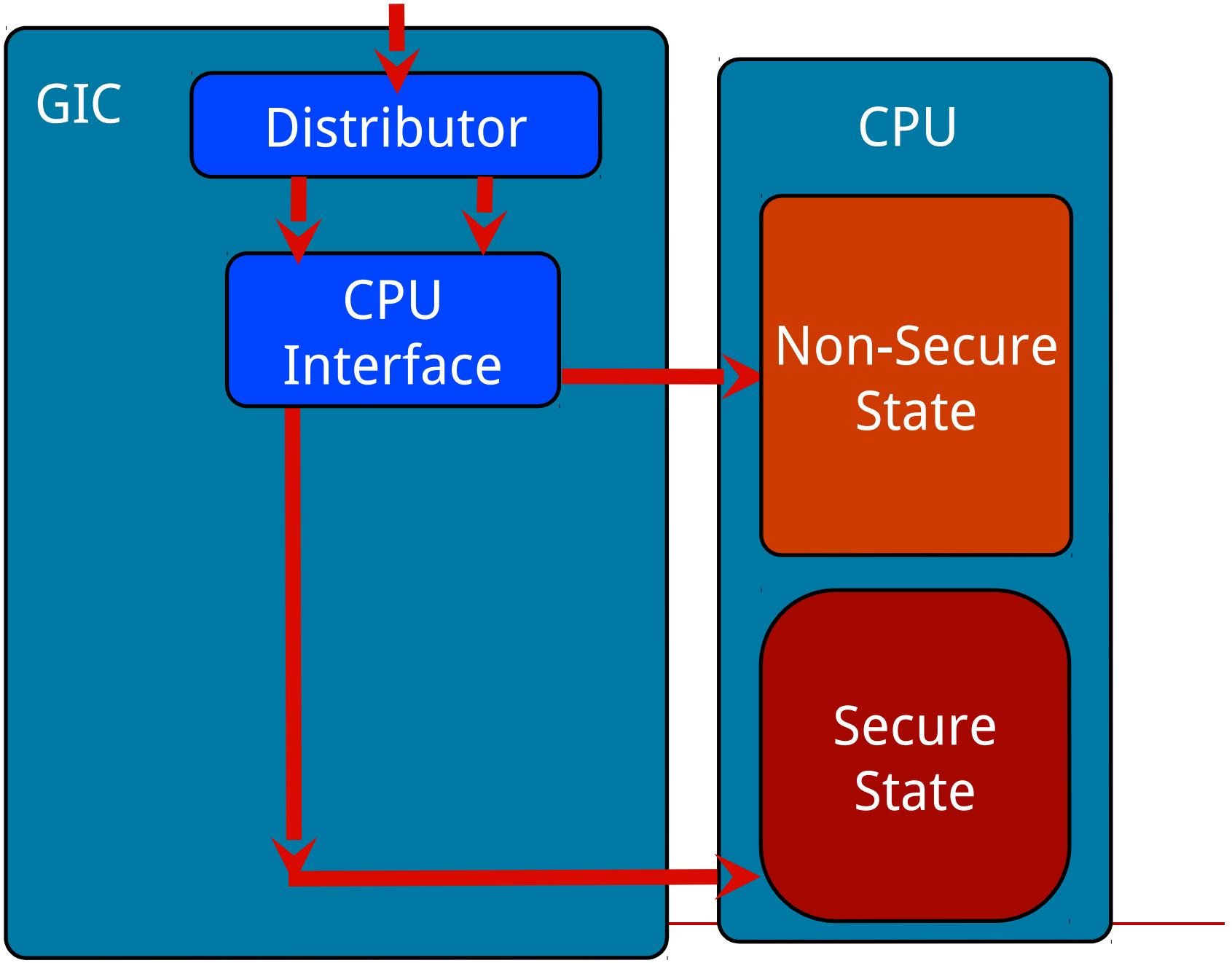
Interrupt Controller

- **MPCore processors include an integrated Interrupt Controller (IC)**
  - Implementation of the Generic Interrupt Controller (GIC) architecture
- **The IC provides:**
  - Configurable number of external interrupts (max 224)
  - Interrupt prioritization and pre-emption
  - Interrupt routing to different cores
- **Enabled per CPU**
  - When not enabled, that CPU will use legacy nIRQ[n] and nFIQ[n] signals



Generic Interrupt Controller

- GIC is the only one interrupt controller in ARM architecture.
- There is a firmware, called “Interrupt Distributor”.
- In Interrupt Distributor, it save the information that which kinds of interrupt should be routed into which kind of state.
- Interrupt distributor should be setting in booting time. Then, we don’t need to take care about GIC.


GIC
Distributor
CPU Interface
CPU
Non-Secure State
Secure State

GIC note

- 每個中斷來源，都可設定優先級，以及當該中斷發生時，哪些處理器要收到該中斷要求
  - 在硬體支援上，會確保一個發送給多處理器的中斷，一次只有一個處理器在處理
- Cortex A9 的 Interrupt Distributor 支援 224 個中斷來源，每個中斷源都有唯一的 ID 識別
  - Software Generated Interrupts (SGI) 用於 IPI
  - 每個 MPCore 中的處理器都會有 Private Interrupt 範圍從 ID0 到 ID15，且只能由軟體觸發中斷
  - 中斷的優先級，會由每個接收中斷的處理器自行設定決定，發出中斷的處理器無法決定接收端的優先級